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## REMARKS/DISCUSSION OF ISSUES

### **Status of the Claims**

Claims 9-29 are pending in the present application, with claims 9-17 withdrawn from consideration at this time. Claim 18 is the independent claim under present consideration.

### **Rejections**

1. Claims 18-20 and 22-25 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Applicant's Prior Art Drawings* in view of *Fukui, et al.* (U.S. Patent 6,100,594) and *Park et al.* (U.S. Publication No. 2002/0089043). For the reasons set forth below, it is respectfully submitted that independent claim 18, and the claims that depend directly or indirectly therefrom are allowable over the applied references.

The establishment of a *prima facie* case of obviousness requires that *all* of the elements be found in the prior art. It follows, therefore, if a single element is not found in the prior art, a *prima facie* case of obviousness cannot properly be established. Moreover, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is a teaching, suggestion or motivation to do so found in the references relied upon. However, hindsight is never an appropriate motivation for combining references and/or the requisite knowledge available to one having ordinary skill in the art. To this end, relying upon hindsight knowledge of applicants' disclosure when the prior art does not teach nor suggest such knowledge results in the use of the invention as a template for its own reconstruction. This is wholly improper in the determination of patentability.

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Claim 18 is drawn to a semiconductor device and includes the features:

*“...a semiconductor element having a circuit forming surface...;*

*a wiring disposed on said circuit forming surface and on a side surface of said semiconductor element;...”* and further includes the features:

*“an outer electrode disposed on said exposed surface of said bump electrode and contacting said wiring on said side surface of said semiconductor element.”*

It should be noted that Applicants have referred to the solder ball electrodes of their invention as **outer electrodes** rather than **ball electrodes** since these electrodes tend to alter their shape during the reflow process as clearly set forth in Applicants' disclosure (compare for example Fig. 7(b) and Fig. 7(c)).

It is respectfully submitted that *Applicant's Prior Art Drawings* lacks a disclosure of at least the featured wiring as set forth in claim 18. This deficiency is not cured by the addition of *Fukui et al* and *Park et al*. The Office Action has made a patchwork mosaic of various pieces of prior art based on Applicants' teachings, yet has failed to provide a valid *prima facie cause of obviousness*.

Applicants disclose and claim a semiconductor device which includes, *inter alia*, a) wiring disposed on both the **circuit forming surface and on a side surface** of the semiconductor element, b) a bump electrode **connected to said wiring and having an exposed surface**, and c) an outer electrode which is both **disposed on said exposed surface of said bump electrode and contacting said wiring on said side surface** of the semiconductor element. This configuration provides the advantages described in Applicants' disclosure, such as multilayering, high-density mounting, and electrical connection between the outer electrodes disposed on the side surfaces of adjacent elements. These advantages cannot be achieved by the prior art references cited by the Examiner, whether taken alone or in combination.

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The Examiner relies on the newly cited *Park et al.* reference for a teaching of wiring disposed on both the circuit forming surface and the side of the semiconductor element. This isolated teaching is not properly combinable with the other references since there is no disclosure in *Park et al.* as to how the wiring 30 would interact with a bump electrode. In fact, wiring 30 could not interact with a bump electrode or an outer electrode because it is covered by insulating layer 40 (see Fig. 3 for example.) Combining *Park et al.* as proposed by the Examiner would be improper and directly contrary to *Park et al.*'s teaching.

Nowhere in the art applied by the Examiner, either taken alone or in combination, is there a teaching of a semiconductor device as described and claimed by Applicants. The provision of a device which combines the illustrative feature as enumerated above, namely wiring on both the circuit forming surface and the side surface of the semiconductor element, a bump electrode connected to the wiring and having an exposed surface, and an outer electrode disposed on the bump electrode and contacting the wiring on the side surface. This structure allows for electrical connection with another element to be achieved at a side surface, and this teaching is not found in the references of record.

Accordingly, for the reasons set forth above, it is respectfully submitted that the applied art fails to disclose the features of claim 18. As such, a *prima facie* case has not been properly established. Therefore, and while in no way conceding as to the propriety of the rejection, or the propriety of the combination of references, it is respectfully submitted that independent claim 18, and the claims that depend directly or indirectly therefrom are allowable over the applied art. Allowance is earnestly solicited.

The additional references cited by the Examiner do not cure the above deficiencies. *Fukui et al.* discloses sealing material 8 with semiconductor chips 1 and 2, but there is no disclosure or suggestion as to how such sealing material could be incorporated into a structure such as claimed by Applicants. *Mori* discloses a

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structure similar to *Fukui et al.* and does not provide any teaching which could be combinable with the other cited references to meet the terms of Applicants' claimed invention. *Ohuchi et al.* does not disclose a ball electrode **disposed on said wiring on said side surface of the semiconductor element** as asserted by the Examiner. In fact, such a structure would not be possible in *Ohuchi et al.* since this reference does not disclose any wiring on the side surface of the semiconductor element. For these reasons, claim 18 and its dependent claims 19-27 are believed to be clearly allowable and such action is solicited.

Newly presented claims 28 and 29 add the feature that the circuit forming surface of the semiconductor device is sealed. This feature, when combined with the limitations of parent claim 18, sets forth structure which also clearly distinguishes from the art of record and therefore allowance of these claims is also respectfully requested.

### ***Conclusion***

In view of the foregoing, applicants respectfully request that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Petition is hereby made for a one-month extension of time as provided under 37 C.F.R. § 1.136(a), extending the period of response from March 5, 2004 to April 5, 2004. Permission is hereby given to charge Deposit Account Number 50-0238 for the required fee under 37 C.F.R. § 1.17.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees, including but not limited to, fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:  
Oki Electric Industry Co. Ltd.



William S. Francos, Esq.  
Reg. No. 38,456

Date: April 5, 2004

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